Abstract

The circuit arrangement wherein the circuit arrangement includes at least one further multiplicity of first adder circuits which follow the multiplicity of first adder circuits the at least one further multiplicity of first adder circuits in each case being supplied with a further error signal vector and the at least one further multiplicity of first adder circuits adding the respective further error signal vector to the at least one signal vector in order to generate a progressively error-corrected signal vector. The circuit arrangement further includes at least one further multiplicity of first multiplier circuits which precede the at least one further multiplicity of first adder circuits and multiply the respective further error signal vector by adjustable coefficients.